AF/JFW

Docket No.: P2001,0134

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MAIL STOP: APPEAL BRIEF-PATENTS

By: /Yongkang Chen/ Date: January 30, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/649,411 Confirmation No.: 5308
Inventor	:	Heike Drummer, et al.
Filed	:	August 27, 2003
Title	:	Process for Producing and Removing a Mask Layer
TC/A.U.	:	1765
Examiner	:	Kin Chan Chen
Customer No.	:	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated October 4, 2005, finally rejecting claims 1-7.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $500.00 to cover the fee for filing the *Brief on Appeal*.

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Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-7 are rejected and are under appeal. Claims 8-14 have been withdrawn. Claim 15 was added in an amendment dated August 24, 2005 and is allowed.

Status of Amendments:

No claims were amended after the final Office action. *A Notice of Appeal* was filed on November 30, 2005.

Summary of the Claimed Subject Matter:

The invention of the instant application relates to a process for producing a mask layer for a semiconductor substrate. The process includes the following steps: providing a configuration including a semiconductor substrate (1), a first layer configuration (2) configured on the semiconductor

substrate, a second layer (3) configured on the first layer configuration, and a third layer (4) configured on the second layer, the first layer configuration being a ferroelectric or dielectric layer configuration of a plurality of individual layers including an upper layer (21) having a metal, a middle layer (22) having barium-strontium-titanate, and a lower layer (23) having iridium or iridium oxide; patterning the third layer (4) to form a first trench (5), which uncovers the second layer, in the third layer; using the third layer (4) as an etching mask, etching the second layer and forming a second trench (6) in the second layer near the first trench, the second trench uncovering the upper layer of the first layer configuration; removing the third layer from the second layer; using the second layer as an etching mask, etching all of the plurality of individual layers of the first layer configuration and forming a third trench (7) in all of the plurality of individual layers of the first layer configuration, the third trench being formed near the second trench and uncovering the substrate; after forming the third trench, depositing a fourth layer (8) of an insulating material on the semiconductor substrate; chemically-mechanically polishing the fourth layer and then the second layer to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer configuration, the fourth layer remaining in place

in the third trench. See page 9, line 6 to page 11, line 13 and page 14, line 2 to page 16, line 17 of the specification.

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 1-7 are obvious over Hirota et al. (US 6,316,329 B1) in view Nishioka et al. (US 5,489,548) or Vaartstra (US 6,225,237 B1) under 35 U.S.C. §103(a).

2. Whether or not claims 1-7 are obvious over Clevenger et al. (US 6,348,395 B1) in view of Nishioka et al. or Vaartstra under 35 U.S.C. §103(a).

Argument:

Claims 1-7 are not obvious over Hirota et al. in view Nishioka et al. or Vaartstra under 35 U.S.C. §103(a).

In item 2 on pages 2-4 of the above-mentioned Office action, claims 1-7 have been rejected as being unpatentable over Hirota et al. in view of Nishioka et al. or Vaartstra under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

providing a configuration including a semiconductor substrate, a first layer configuration configured on the semiconductor substrate, a second layer configured on the first layer configuration, and a third layer configured on the second layer, the first layer configuration being a ferroelectric or dielectric layer configuration of a plurality of individual layers including an upper layer having a metal, a middle layer having barium-strontium-titanate, and a lower layer having iridium or iridium oxide;

patterning the third layer to form a first trench, which uncovers the second layer, in the third layer;

using the third layer as an etching mask, etching the second layer and forming a second trench in the second layer near the first trench, the second trench uncovering the upper layer of the first layer configuration;

removing the third layer from the second layer;

using the second layer as an etching mask, etching all of the plurality of individual layers of the first layer configuration and forming a third trench in all of the plurality of individual layers of the first layer configuration, the third trench being formed near the second trench and uncovering the substrate;

after forming the third trench, depositing a fourth layer of an insulating material on the semiconductor substrate;

chemically-mechanically polishing the fourth layer and then the second layer to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer configuration, the fourth layer remaining in place in the third trench.

According to claim 1, the invention of the instant application relates to a process in which a layer stack including layers (21, 22, 23) is to be etched with respect to a hard mask layer (3). The layer stack (21, 22, 23) includes an upper layer including metal, a middle layer including barium-strontium-titanate or strontium-bismuth-tantalate, and a lower layer

including iridium or iridium oxide. Having etched the layer stack (21, 22, 23), the corresponding trench is filled with a fourth layer (8) of an insulating material. Then, the fourth layer is removed and the second layer is removed (which is the hard mask). This results in a structure as shown in Fig. 6, where the layer (2) of Fig. 6 is actually a layer stack including layers similar to the layers (21, 22, 23) of Fig. 7.

Applicants believe that the Examiner has taken a very formalistic approach when he attempts to combine the teachings of Hirota et al. and Nishioka et al. or Vaartstra. Applicants believe that Hirota et al., on one hand, and Nishioka et al. and Vaartstra, on the other hand, relate to different processes and there is no link between them which would encourage a person skilled in the art to transfer the technical teaching from Nishioka et al. or Vaartstra to Hirota et al., for the reasons that are discussed below.

Hirota et al. describe the formation of shallow trench isolation (see Figs. 3C - 3G). The layer stack 102, 103, 104 to be etched includes silicon oxide 102, diamond-like carbon 103, and amorphous silicon 104 (see column 6, first paragraph).

Nishioka et al. in fact describe a ferroelectric layer stack including layers 42, 44, 46, for example made of iridium, barium-strontium-titanate, platinum (see the table in column 9). It becomes apparent from Fig. 12 that the only layer to be patterned is the lower layer 42. The middle and the upper layers 44 and 46, respectively, are continuous layers practically covering the full wafer, a portion of which is shown in Fig. 12. At least, Fig. 12 does not show that layers 44 and 46 would have to be patterned. Thus, a person skilled in the art would not be encouraged to use the layer stack 42, 44, 46 of Nishioka et al. in the environment of Hirota et al. As is clearly shown in Hirota et al., all three layers 102, 103, 104 are patterned and removed within the trench 110 to be etched, while layers 44 and 46 of Nishioka et al. must not be etched.

A layer stack including metal, barium-strontium-titanate or strontium-bismuth-tantalate and another layer of iridium or iridium oxide is known to a person skilled in the art. Nothing else is disclosed in Nishioka et al. However, the invention of the instant application claims the etching of all three layers 21, 22, 23, the coverage with a fourth layer of isolation material, and the subsequent processing by CMP. Nishioka et al. provide no hint to use the layer stack 42,

44, 46 in the shallow trench isolation structure of Hirota et al.

Vaartstra describes a ferroelectric capacitor (Fig. 1) where the capacitor layer stack of layers 13, 11, 12 is patterned. However, while the invention of the instant application claims a CMP process wherein the fourth layer and the hard mask etching layer are chemically-mechanically polished, such a process step cannot be determined in connection with Fig. 1 of Vaartstra since the isolating layer (no reference symbol available), which covers layer stack 13, 11, 12, covers layer 12 and extends beyond layer 12 so that it is not planarized with layer 12. Planarization, however, is the case in Fig. 3G of Hirota et al. as well as in Fig. 6 of the invention of the instant application. Applicants, therefore, believe that a person skilled in the art would not be encouraged to use the teaching of Vaartstra in the environment of Hirota et al.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 2-7 are dependent on claim 1, they are believed to be patentable as well.

Claims 1-7 are not obvious over Clevenger et al. in view Nishioka et al. or Vaartstra under 35 U.S.C. §103(a).

In item 3 on pages 4-5 of the above-mentioned Office action, claims 1-7 have been rejected as being unpatentable over Clevenger et al. (US 6,348,395 B1) in view of Nishioka et al. or Vaartstra under 35 U.S.C. § 103(a).

As already discussed above, according to claim 1, the invention of the instant application relates to a process in which a layer stack including layers (21, 22, 23) is to be etched with respect to a hard mask layer (3). The layer stack (21, 22, 23) includes an upper layer including metal, a middle layer including barium-strontium-titanate or strontium-bismuth-tantalate, and a lower layer including iridium or iridium oxide. Having etched the layer stack (21, 22, 23), the corresponding trench is filled with a fourth layer (8) of an insulating material. Then, the fourth layer is removed and the second layer is removed (which is the hard mask). This results in a structure as shown in Fig. 6, where the layer (2) of Fig. 6 is actually a layer stack including layers similar to the layers (21, 22, 23) of Fig. 7.

Applicants believe that the Examiner has taken a very formalistic approach when he attempts to combine the teachings of Clevenger et al. and Nishioka et al or Vaartstra. Applicants believe that Clevenger et al., on one hand, and Nishioka et al. and Vaartstra, on the other hand, relate to different processes and there is no link between them which would encourage a person skilled in the art to transfer the technical teaching from Nishioka et al. or Vaartstra to Clevenger et al., for the reasons that are discussed below.

Clevenger et al. disclose a process (Figs. 3A to 3D) similar to the process disclosed in Hirota et al. For example, the layer 260 may be silicon-germanium, the layer 270 may be an oxide layer, and the layer 220 may be diamond-like material. All of this is not the claimed layer stack of the invention of the instant application, which includes metal, barium-strontium-titanate or strontium-bismuth-tantalate and iridium or iridium oxide according to claim 1 of the instant application. Hence, the arguments as set forth above relating to Hirota et al., Nishioka et al., and Vaartstra apply to the rejection relating to Clevenger et al., Nishioka et al., and Vaartstra in a similar way.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either

show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 2-7 are dependent on claim 1, they are believed to be patentable as well.

In addition, Applicants note that Hirota et al. and Clevenger et al. both refer to the simultaneous removal and planarizing of a filling layer including a hard mask. However, Hirota et al. and Clevenger et al. use an additional layer which is a diamond-like layer (layer 103 in Hirota et al.; layer 220 in Clevenger et al.). This is an additional layer, which must be removed later on due to its nature (e.g. Fig. 31 of Hirota et al.), while layers 21, 22, 23 of the invention of the instant application are maintained as capacitor dielectric.

Nishioka et al. describe a ferroelectric capacitor and describe a high dielectric capacitor material similar to the materials which are also applicable within the invention of the instant application. However, Nishioka et al. do not describe the structuring of such layers through CMP and etching. Nishioka et al. focus on sidewall spacers for a capacitor.

The structure within Hirota et al. and Clevenger et al. on one hand and the structure of Nishioka et al. on the other hand

are incompatible with each other. For example, Applicants believe that a person skilled in the art would not be motivated to replace, e.g. diamond-like carbon in Hirota et al. or Clevenger et al. with the materials from Nishioka et al. In fact, since diamond-like carbon is a polish stop and is not a material usually used as a dielectric material for capacitors, a person skilled in the art would further not be motivated to replace the diamond-like carbon by the high dielectric constant materials disclosed in Nishioka et al.

As to the Examiner's argument in item 4 on page 6 of the final Office action, it is noted that the Examiner did not substantiate how the suggestion or motivation for combining the teachings of the cited prior art references could be found in the references themselves or in the knowledge generally available to a person skilled in the art. As discussed above, Applicants believe that the structures and the intentions of the references are not compatible with each other so that a combination or modification is not suggested although several of the materials used in the invention of the instant application are known to a person skilled in the art.

In view of the forgoing, the honorable Board is therefore

respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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Claims Appendix:

1. A process for producing a mask layer for a semiconductor substrate, the process which comprises:

providing a configuration including a semiconductor substrate, a first layer configuration configured on the semiconductor substrate, a second layer configured on the first layer configuration, and a third layer configured on the second layer, the first layer configuration being a ferroelectric or dielectric layer configuration of a plurality of individual layers including an upper layer having a metal, a middle layer having barium-strontium-titanate, and a lower layer having iridium or iridium oxide;

patterning the third layer to form a first trench, which uncovers the second layer, in the third layer;

using the third layer as an etching mask, etching the second layer and forming a second trench in the second layer near the first trench, the second trench uncovering the upper layer of the first layer configuration;

removing the third layer from the second layer;

using the second layer as an etching mask, etching all of the plurality of individual layers of the first layer configuration and forming a third trench in all of the plurality of individual layers of the first layer configuration, the third trench being formed near the second trench and uncovering the substrate;

after forming the third trench, depositing a fourth layer of an insulating material on the semiconductor substrate;

chemically-mechanically polishing the fourth layer and then the second layer to remove the fourth layer from the second layer and then to remove the second layer from the upper layer of the first layer configuration, the fourth layer remaining in place in the third trench.

2. The process according to claim 1, wherein the upper layer of the first layer arrangement includes tungsten, tantalum, titanium, copper, titanium nitride, tantalum nitride, tungsten silicide, tungsten nitride, platinum, iridium, cobalt, palladium, silicide, nitride, or carbide.

3. The process according to claim 1, wherein the third layer is a photosensitive mask layer.

4. The process according to claim 1, wherein the fourth layer includes silicon oxide, silicon nitride, butylcyclobutene, or polybutyl oxalate.

5. The process according to claim 1, which further comprises performing the chemically mechanically polishing step using a polishing fluid having a solids content of between 20% and 40%.

6. The process according to claim 1, which further comprises performing the chemically mechanically polishing step using a polishing fluid including ammonia.

7. The process according to claim 1, which further comprises performing the chemically mechanically polishing step using a polishing fluid having a pH between 9 and 11.

Evidence Appendix:

No evidence pursuant to && 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

Since there are no prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, no copies of decision rendered by a court or the Board are available.